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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Applicant	:	Stephen R. Van Doren, et al.
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For	:	SYSTEM AND METHOD TO FACILITATE ORDERING POINT MIGRATION TO MEMORY
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REPLY BRIEF

Sir:

This Reply Brief is in response to the Examiner's Answer dated January 31, 2008 (hereinafter, "Examiner's Answer"). This Reply Brief addresses the Examiner's Answer concerning the appealed claims 1-7 and 9-30.

Preliminary Comments:

Appellant's Amended Appeal Brief dated November 30, 2007 (hereinafter, "Appeal Brief"), addresses the issues raised in the Grounds of Rejection beginning at Page 3, line 3, of the Examiner's Answer. Accordingly, this reply brief focuses on certain statements made in the Response to Argument section, beginning at page 10, line 5 of the Examiner's Answer.

Prior to addressing the substance of the Examiner's Answer, Appellant respectfully points out that a rejection for anticipation under section 102 requires that each and every limitation of the claimed invention be disclosed in a single prior art reference." *In re Paulsen,* 30 F.3d 1475, 1478-79 (Fed. Cir. 1994). While this is well settled, the Examiner's Answer leads down a path of comparing portions of Appellant's specification relative to cited references but fails to consider each and every limitation of what is being claimed.

Appealed Claim 1:

In view of the foregoing, it is helpful to understand the structural and functional interrelationships recited in claim 1. Respectfully, claim 1 recites a first node that is operative to employ a write-back transaction associated with writing data back to memory, and also recites that this same first node includes an ordering point for the data. This first node is also recited in claim 1 as broadcasting a write-back message to at least one other node in the system in response to an acknowledgement that has been provided by the memory. This acknowledgement, which is expressly recited as being provided by the memory, indicates that the ordering point for the data has migrated from the first node to the memory. It is this combination of claim features that is not taught or even suggested in Glasco individually or in combination with any other art of record.

The Examiner's Answer as well as the Final Office Action dated March 21, 2007 (hereinafter, "Final Action"), focus on specific language in the specification that is taken out of its context and apart from the other parts and functionality and structure of the system to support a contention that Glasco discloses "claimed subject matter at least in

the manner recited in applicant's specification." Examiner's Answer at page 10, lines 15-17. For example, the Examiner's Answer at page 11, line 4, quotes a statement in Appellant's specification that "a cache line having any one of the state's M, O and D must implement a write-back to memory upon displacement of the associated data." However, this and related statements quoted from Appellant's specification have been removed from the context of that the cache line first is defined as an ordering point in the cache coherency protocol that is implemented in the system being described. Appellant is not simply claiming a write-back transaction for data having an M, O or D state, as it appears to be suggested in the Examiner's Answer. The following table demonstrates a quoted section from the Examiner's Answer at page 11, lines 11 – 17 apparently taken from Glasco at paragraphs [0116, 0120 – 0123].

EXAMINER'S ANSWER QUOTING GLASCO	CLAIM 1
"a system having a cache coherency directory where cache lines have states including modified (M), owned (O), shared (S), dirty (D), and invalid (I). If the directory entry indicates that the line is in the "dirty" state, the modified memory line to memory must first be written back to memory; the eviction of a cache coherency directory entry corresponding to a "dirty" line in a remote cache requires that the remote cache writes the line back to memory."	A system comprising: a first node that includes an ordering point for data, the first node being operative to employ a write-back transaction associated with writing the data back to memory, the first node broadcasting a write-back message to at least one other node in the system in response to an acknowledgement provided by the memory indicating that the ordering point for the data has migrated from the first node to the memory.

Firstly appellant objects to the contention that the quoted language is actually a quotation from Glasco as represented in the Examiner's Answer. In particular, the quote from the Examiner's Answer includes incomplete sentences taken from several different paragraphs out of their context and inserted there seemingly as a complete thought in the Examiner's Answer. Instead, this quote is best characterized as the Examiner's own collection and arrangement of information from these paragraphs of Glasco. In fact, the portion extracted from paragraph [0116] states that if the directory entry indicates that the line is in the "dirty" state in any of the remote caches, the

modified memory line to memory must first be written back to memory **before the line is invalidated**." See Glasco at paragraph 116, lines 5–9.

Additionally, a direct comparison between claim 1 and the Examiner's collection of statements from Glasco demonstrates that nowhere in the quoted section of Glasco is there any disclosure that an ordering point for data can migrate from a node to memory as recited in claim 1. In sharp contrast, the quoted section of Glasco simply refers to a traditional write-back transaction in which a memory line is written back to memory before it is invalidated in conjunction with a sized write transaction. Glasco at para. [0118]-[0119].

There is further no evidence in Glasco that supports the Examiner's contention that an ordering point for a given cache line migrating to memory, as recited in claim 1. Instead, the Examiner's attempting to conclude that since the present specification describes a certain function associated with a cache line must occur that such same function most also occur in a write-back transaction in the context of Glasco. This, however, demonstrates application of faulty logic in the Examiner's Answer, which upon consideration of what is disclosed in Glasco, reveals a significant difference between the approach in Glasco and that recited in the system of claim 1. The Examiner's Answer at page 11, line 17 – 22, concludes that simply because Glasco discloses a write-back transaction to memory that an ordering point is migrating for a given cache line, from cache to memory. What is being claimed does not correspond to a normal or inherent property of a state of a cache line, but a condition set upon the cache line by the particular cache coherency protocol being implemented in the overall system. In fact, examples of serialization points for a single cluster system in a multiple processor multiple cluster system are described in Glasco at paragraphs [0045] to [0046], none of which mentions any basis or support for the proposition in the Examiner's Answer, that an ordering point would migrate from cache to memory.

At page 13, lines 7 – 13, the Examiner's Answer states that:

> "the Examiner simply applies verbiage of the proposed claim the broadest reasonable meaning of their words in their ordinary usage as they would be understood of one of ordinary skill in the art taken into account whatever enlightening by way of definitions or otherwise that may be afforded by the written description contained in applicant's

> specification." Citing *In re Morris*, 127 F.3d 1048, 1054 – 55, 44 U.S.P.Q.2d 1023, 1027 – 1028 (Fed. Cir. 1997).

Appellant submits that the Examiner's Answer has gone well beyond the holding of *In re Morris*. Appellant does not dispute that some cases state the standard for claim interpretation is "the broadest reasonable interpretation," *see, e.g., In re Van Geuns*, 988 F.2d 1181, 1184, 26 U.S.P.Q.2D (BNA) 1057, 1059 (Fed. Cir. 1993), and that other cases include the qualifier "consistent with the specification" or similar language, *see, e.g., In re Bond*, 910 F.2d 831, 833, 15 U.S.P.Q.2D (BNA) 1566, 1567 (Fed. Cir. 1990). What Appellant strongly objects to is the deficiency of the evidence being relied on in the Examiner's Answer from Glasco relative to what is claimed and the resulting conclusion.

As discussed above, the focus by the Examiner to the specific section in Appellant's specification concentrates on a single isolated example with a particular set of circumstances that fails to consider the particular context and other information associated with the quoted section that relates to other features being claimed. The Examiner concludes that certain claimed features are disclosed in Glasco because of the similarities in the types of transaction and the type of states that are being described. This rationale appears to presume that all cache coherency protocols that might include similar states and utilize same types of transactions must operate in the same manner. This is faulty reasoning that is unsupported in the law and is inconsistent with the teachings of Glasco.

Significantly, Appellant respectfully argued in its Appeal Brief that a memory controller in Glasco remains a serialization point for the memory line before, during and after writing back to memory. In response, beginning at page 13, penultimate line, the Examiner's Answer states:

> "...Glasco neither in those paragraphs point to by applicants nor anywhere else teaches that "a given memory controller remains the serialization point for the memory line before, during and after writing back to memory as alleged by applicants." (Emphasis in original).

However, Glasco expressly discloses that "memory controllers of the multi cluster architecture described herein act as serialization points for memory transactions. That

is, once a memory controller accepts a transaction for one of its memory lines, it blocks all other transactions to that same memory line. Therefore, once the home memory controller accesses the sized write transaction, it does not allow any further transactions for the same memory line until the eviction process is completed." Glasco at para. [0127]. Applicant submits that Glasco does expressly teach that the home memory controller for the same memory line is the serialization point before the eviction process as well as after the eviction process is completed, as Appellant stated in its Appeal Brief. Additionally, while the home memory controller (i.e., the serialization point) does not accept further transactions once it accepts a transaction for one of its lines, the home memory controller nonetheless remains the serialization point for the same memory line. Glasco at para. [0127]. Stated differently, since the home memory controller does not allow further transactions until the eviction process is completed, it logically follows that after the eviction process has been completed (writing the cache line back to memory), the home memory controller (still the ordering point) would once again then allow transactions for that same memory line. Therefore, applicant statements are true and accurate based upon the express teachings of Glasco. Again, the differences between claim 1 and the approach in Glasco results from the use of significantly different types of coherency protocols.

Beginning at page 14, line 13, the Examiner's Answer states that:

> "Glasco clearly discloses 'in a cluster system requests are generated to specific processors to invalidate cache entries and to write cache entries back to memory; if the directory entry indicates that the line is in the **dirty (D) state** in any of the remote caches the modified memory line to memory **must first be written back** before the line is invalidated in each of the remote caches; Paragraphs [0116, 0118, 0120]'."

Firstly, Appellant objects to the use of quotations in the Examiner's Answer for the sections in Glasco. Significantly, the first clause does not exist in any of the cited paragraphs of Glasco. Additionally, the second clause is not an exact quotation, and at best is a vague paraphrase of what is disclosed in Glasco which does not appear to be disclosed in any of the cited paragraphs. Moreover, the sections are, at most, the Examiner's own collection of statements taken out of context from Glasco and arranged

as a single thought. Thus, the use of quotation marks in the Examiner's Answer is inaccurate and misleading.

The Examiner again makes improper usage of quotation marks at page 15, lines 6–9, in alleging that Glasco teaches "...sending invalidation messages to each of the remote caches in a cluster system if the directory entry indicates that the line is in the dirty state (D) and the modified line must be written back to memory". In addition to not providing any citation to Glasco's alleged teaching, the Examiner's Answer alleges fact that it is in great dispute. Additionally, the Examiner's Answer states that this purported teaching of Glasco "provides acknowledgement that the ordering point has migrated from a node to memory." Examiner's Answer, page 15, lines 9-10. As discussed above, there is no basis to conclude that an ordering point migrates in the allegedly quoted section from Glasco or elsewhere in Glasco in conjunction with a write-back to memory. In fact, as discussed above, Glasco explicitly teaches that the home memory controller will remain the serialization point for the given memory line that is being evicted through the write-back transaction at least before and after the transaction. See Glasco Paragraph [0127].

Additionally, the proposition fails to appreciate that claim 1 also recites that the first node (which includes the ordering point that migrates to the memory) also broadcasts a write-back message to at least one other node. This write-back message is broadcast by the first node, significantly, in response to an acknowledgement that is provided by the memory indicating that the ordering point has migrated from the first node to the memory. However, the alleged teaching from Glasco (Examiner's Answer at page 15, lines 6–9) when considered in its intended context demonstrates that the conclusion reached by the Examiner in the Examiner's Answer and in the Final Action is not supported by evidence. For instance, Glasco teaches that the home memory controller (the serialization point) receives a dirty copy of memory line and performs a NOP write speed line back to memory and notifies the cache coherence directory that the transaction is complete, but the home memory controller remains the serialization point for the reasons discussed above. See Glasco at paragraph [0126] and [0127].

Again, as mentioned above, these differences result from the diverse protocols being implemented in the approach of Glasco and in the system of claim 1.

Appealed Claim 2

Appellant respectfully argued in its Appeal Brief, page 19, that Glasco fails to disclose the system of claim 2. In response to these arguments, the Examiner's Answer, beginning at page 15, line 6, contends that claim 2 is anticipated by Glasco. The following table compares a quote from the Examiner's Answer, at page 15, lines 6-10, relative to claim 2.

EXAMINER'S ANSWER QUOTING GLASCO	CLAIM 2
"If a directory indicates that the line is in a "dirty" state (D) in any of the remote caches, the modified memory line to memory must first be written back to memory; the eviction of a cache coherency directory entry corresponding to a "dirty" (D) line in a remote cache requires that the remote cache write the line back to memory:' pars. [0116, 0120]	The system of claim 1, wherein the first node comprises a processor having an associated cache that comprises a plurality of cache lines, one of the plurality of cache lines having an associated state that defines the cache line as a cache ordering point for the data prior to employing the write-back transaction.

From the side-by-side comparison of the reliance on Glasco in the Examiner's Answer relative to claim 2, it is evident that the quoted sections from Glasco fails to include any description relating to that a state of a cache defines a cache line of the first node (claim 1) as a cache ordering point for data prior to employing a write-back transaction, as recited in claim 2. The basis for the conclusion in the Examiner's Answer again appears to be a focus to a description in the Appellant's specification at paragraph [0028]. However, a quoted section of applicant's specification taken out of its context and away from structure and function that is also recited in the claim fails to provide sufficient support for an anticipation rejection since the quoted section of Glasco fails to include features and relationships associated with the system of claim 2.

At page 16, line 17, through page 17, line 3, the Examiner's Answer inaccurately purports to reproduce statements from Appellant's Response that was filed on December 20, 2006. In particular, the Examiner's Answer alleges that appellant affirms or attests to certain teachings of Glasco citing to Page 9, paragraph 1 of Appellant's Response that was filed on December 20, 2006. Submitted herewith as Exhibit 1 is

page 9 of Appellant's response filed on December 20, 2006. In the attached Exhibit A, the quoted section in the Examiner's Answer (which appears to be from the last paragraph of page 9) has been highlighted in its entirety. Exhibit A demonstrates that Appellant clearly stated that Glasco **fails** to disclose the subject matter of claim 2 and demonstrating an obvious mischaracterization by the Examiner of Appellant's prior remarks.

At page 17, beginning at line 11 the Examiner's Answer states "Examiner simply made use of a well know practice of Patent Examination and Prosecution by interpreting the claims as broadly as their terms reasonably allow, in light of "the present specification", which is not impermissible reliance on the application's specification and applicants' disclosed embodiments are best suitable in interpreting the claimed invention." However, in the instant situation, the Examiner is not simply interpreting the claims in light of the specification but is attempting to read the present specification on a disclosure from the reference to support its rejection. Appellant has demonstrated that the purported teachings of Glasco being relied on in the Examiner's Answer and in the Final Action fails to teach each and every element of claim Moreover, as discussed above, the quoted section from Appellant's specification is taken out of its context and therefore does not constitute a proper basis for interpretation of what is recited in claim 2. Thus, from the comparison above it is demonstrated that the quoted section of Glasco is deficient in teaching what is recited in claim 2. Therefore, claim 2 is not anticipated by Glasco.

Appealed claim 3:

Regarding claim 3, the Examiner's Answer contends that arguments on page 20, paragraph 2 of Appellant's remarks are erroneous. The Examiner's basis for its contention cites to a section from paragraph [0126] of Glasco, which is reproduced in the table below adjacent claim 3 for comparison.

EXAMINER'S ANSWER QUOTING GLASCO	CLAIM 3
"a home controller (one other node) receives the "dirty" copy of the memory line, writes the line back to memory and notifies the cache coherence directory (i.e., the originator of the transaction or first node) that the transaction is complete"; par. [0126].	The system of claim 1 wherein the at least one other node provides a response to the first node acknowledging receipt of the write-back message broadcast by the first node.

Claim 3 depends from claim 1 and thus includes all of the subject matter of claim 1 in addition to what is recited in claim 3. The above-quoted section in the table states that the cache coherence directory is the node that originated the transaction, which in claim 1 from which claim 3 depend corresponds to the first node. However, as discussed above, the cache coherence directory is not the ordering point for the data but instead the home memory controller is the serialization point. See Glasco at paragraph [0127]. Additionally, the home memory controller writes the line back to memory and notifies the cache coherence directory of such writing back. Glasco at paragraph [0126]. In contrast to what is recited in claim 1 from which claim 3 depends, however, the cache coherence directory of Glasco does not broadcast a write-back message to at least one other node in the system, as recited in claim 1. Consequently, the home controller of Glasco does not provide a response that acknowledges receipt of a write-back message that has been broadcast by any cache coherence directory as suggested in the Examiner's Answer.

The Examiner's Answer further refers to paragraph [0049] of Glasco to support a contention that a cache coherence directory broadcast a write-back message. Examiner's Answer, ultimate paragraph. However, the reliance of paragraph [0049] of Glasco is being taken out of its intended context and contrary to the description at Glasco at paragraph [0124] which is relied upon to support the Examiner's rejection of claim 3. In particular, the implementation being described at paragraph [0124] includes a cache coherence directory, which does not employ the broadcast probes as is done in the typical implementation described in the first three sentences of [0049]. Instead, the coherence directory is used to reduce the number of probes to remote quads by

inferring the states of local caches. See ultimate sentence of paragraph [0049] of Glasco. Thus, in paragraph [0124] of Glasco the mention of the cache coherence directory directing the request to the local memory controller is not a broadcast as alleged in the Examiner's Answer, but instead is a point-to-point request that is only directed to the local memory controller for the memory line (i.e., the home memory controller). Moreover as discussed above, this home memory controller for the given line is a serialization point that remains fixed before a transaction and after a transaction is completed including an eviction transaction. See Glasco at paragraph [0127].

Appellant respectfully argued in its Appeal Brief that "the originator of the transaction (the cache coherence controller in the home cluster - see Glasco Par. [0124]) does not broadcast a write back message, as recited in claim 1, from which claim 3 depends." At page 19, beginning at line 8, the Examiner's Answer responded by stating that:

> "Additionally, in response to applicant's argument that the references fail the show "the originator (home node) of the transaction does not broadcast a write-back message", it is noted that the features upon which applicant relies (i.e., "the originator (home node) of the transaction does not broadcast a write-back message") are not recited in the rejected claim(s). The claims simply recite "...***one other node*** broadcasting a write-back message..."

However this set of statements fails to appreciate that claim 3 depends from claim 1 and as such functions and structures of the first node from claim 1 are also included in the system of claim 3. That is, claim 1 expressly recites that the first node, which is operative to employ the write-back transaction, broadcasts the write-back message to at least one other node in the system in response to an acknowledgement provided by the memory... Additionally applicant objects to the particular quotation where the Examiner's Answer states that the claims simply recite "...***one other node*** broadcasting a write-back message...", whereas claim 1 explicitly recites that the first node broadcasts the write-back message. Thus, it is understood that one of the plurality of cache lines of the processor of the first node has the state that defines the cache line of the cache ordering point of the data prior to (the first node) employing the write-back transaction in marked contrast to the teachings of Glasco.

Appealed claim 4:

Appellant's Appeal Brief respectfully argued that Glasco fails to disclose claim 4. In response, the Examiner's Answer alleges support is found in Glasco, citing several paragraphs. A quotation from the Examiner's Answer, at page 29, lines 3-8, to support the Examiner's allegation is reproduced in the table below adjacent claim 4 for comparison.

EXAMINER'S ANSWER QUOTING GLASCO	CLAIM 4
"Glasco clearly discloses "a write-back is generated for the cached memory line; the copy of the line in the cache is invalidated and the eviction mechanism is notified when the memory line has been written back to memory; once the memory controller accepts the sized write transaction, it does not allow any further transactions for the same memory line until the eviction process is completed"; pars. [0121-0123, 0127]."	The system of claim 3, wherein the first node maintains the write-back transaction active until the first node receives responses from the at least one other node to the write-back message broadcast by the first node.

A side-by-side comparison above clearly demonstrates that the quoted sections of Glasco fail to support the allegation that the transaction remains active until the first node receives responses from at least one other node to the write-back message that has been broadcast by the first node. Regardless of whether the home memory controller would accept or allow further transactions for the same memory line until the eviction process is completed, there is nothing in the quoted section to demonstrate that the eviction process includes mention of the circumstances that cause the home controller to maintain a write-back transaction active, as recited in claim 4. The above-quoted language from the Examiner's Answer seems to indicate that the Examiner has confused and intermingled functions of the coherence directory and the memory controller, which operates as the serialization point in the system of Glasco.

Appealed claim 9:

The Examiner's Answer on page 20, beginning at line 13 repeats the arguments made with respect to claim 1 to support its rejection of claim 9. It is noted that independent claim 9 does not simply recite the use of a write-back transaction as is being described in the quoted sections of Glasco. In contrast to Glasco, claim 9 recites that the memory provides an acknowledgement back to the first processor (that provides a write-back request) in response to the write-back request. Moreover, the first processor of claim 9 provides a source broadcast write-back request to the system in response to the acknowledgement that is provided by the memory. This combination of broadcast messaging, acknowledgments, and requests is not disclosed or suggested in Glasco or any art of record.

This is due to the different coherency protocols described and utilized and the system of Glasco in that of the present application. The Examiner purports to rely on the simple basis of having states in common, modified, owner owned and dirty state and the use of the write-back transaction to necessitate the transfer of an ordering point from cache of a processor to memory in conjunction with implementing a write-back transaction as is recited in the system of claim 9. However, there is nothing to support this contention in Glasco or in the Examiner's Answer. In fact such conclusion can only be based on speculation and a mischaracterization of what is taught in Glasco relative to claim 9. The remaining positions in the Examiner's Answer relative to various claims are simply reiterations of the prior arguments which have been adequately addressed above.

Regarding the rejections of claims 5-6, 8, 10-11, 13, 15, 18-19, 21-22 and 25-28 by Glasco in view of Rollins, Appellant acknowledges the Supreme Court decision of *KSR International Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 82 U.S.P.Q.2d 1385 (2007). Appellant further submits that consistent with the holding of this case, Appellant has and demonstrated in its Appeal Brief and this Reply Brief that significant differences exist between the prior art and what is being claimed. In particular, Glasco fails to teach or suggest any basis for ordering point migration, but instead employs a memory controller that remains a serialization point for a given memory line even after eviction of the given

memory line. See, e.g., Glasco at paragraph [0127]. The Final Action and the Examiner's Answer have failed to articulate any basis or reasoning that any teachings in the prior art can be combined in a predictable manner to provide the system of claim 5 in which the node retries the source broadcast request for the data. The Court in *KSR* has held that "there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness (35 U.S.C. §103)", which is lacking in the Examiner's Answer. *KSR International Co. v. Teleflex Inc.*, supra. Thus, the statement of law set out in the Examiner's Answer at page 27, line 10, through page 28, line 28, regarding obviousness regarding claim 10 and claim 5 appear not to be followed by providing a sufficiently articulated reasoning to support the obviousness rejections.

Regarding claim 18, after quoting a lengthy section from Appellant's specification selected from various paragraphs, the Examiner's Answer, at page 33, lines 12-16, states to support the rejection of claim 18 that:

> Rowlands further discloses "retrying an address transfer to permit a modified cache block to be written to memory, or other coherency activity to occur; [par. 0113]" where it would have been apparent to one of ordinary skill in the art that the step of "retrying" would not be performed indefinitely and would retire at some point."

However neither the quoted section of Rowlands nor Rowlands more generally provides any basis to conclude that the outstanding transaction would be retired in response to receiving acknowledgement of receipt of the source broadcast write-back message as recited in claim 18. Moreover, the source broadcast write-back message is recited in claim 16 from which claim 18 depends. Nowhere in Rowlands is such a write-back message or any mechanism for providing such a write-back message disclosed or suggested in Rowlands or Glasco. Significantly, Rowlands and fails to demonstrate the retiring of a transaction in response to the particular set of conditions recited in claim 18. Therefore, the combination of Glasco and Rowlands fails to make claim 18 obvious.

At page 35, beginning at line 5, the Examiner's Answer alleges that applicant has argued features that are not recited in the rejected claims. However claim 27 (a method claim) clearly recites that the method of claim 23 that further comprises recognizing the conflict associated with the request for the data provided by at least one of the other

nodes. Accordingly, in order for something to perform such function that is recited in the claim something has to perform the function. Appellant's Appeal Brief did assert that particular structure is recited in claim 27. Instead, Appellant respectfully argued that Rowlands fails to teach any structure that can perform the functions that are recited in claim 27 to demonstrate the deficiency in the evidence relied on in the Examiner's Answer and the Final Action. Therefore, since the Final Action and Examiner's Answer have failed to set out an articulated reasoning with some rational underpinning to support the legal conclusion of obviousness, claim 27 is not obvious over the combination of Rowlands and Glasco.

In support of its rejection in claim 28, the Examiner's Answer relies on Glasco at paragraph [0137]. The following table provides side-by-side comparison of a quote from the Examiner's Answer, at page 36, lines 1 – 5 relative to claim 28.

EXAMINER'S ANSWER QUOTING GLASCO	CLAIM 28
Glasco clearly discloses "it is possible that conflicting transactions may be generated (i.e., recognized by the originator node) during the time between when the cache coherence directory to evict (write-back) a particular entry and the corresponding request is received by the memory controller (i.e., third node); par. [0137].	The method of claim 27, wherein the request for the data provide by the at least one of the other nodes comprises a source broadcast request, the recognizing of the conflict further comprising recognizing the conflict in response to one of (i) receiving the source broadcast write-back request provided by the first processor node while the source-broadcast request for the data is outstanding at the at least one of the other nodes, or (ii) receiving a conflict response from the first node to a source broadcast request issued by the at least one of the other nodes.

First, the quoted section from paragraph [0137] of Glasco does not teach or suggest a source broadcast write-back request, but instead is a directory entry in which transactions are sent more directly to the memory controller through point-to-point connection. Moreover the quoted section of Glasco has no basis that the recognition of a conflict in response to either of the particular conditions recited in claim 28. The fact

that conflicting transactions may be generated or exist in the approach to Glasco does not amount to any recognition of the conflict, especially not a recognition in response to the particular conditions recited in claim 28. For this reason there is not sufficient evidence to find claim 28 obvious in view of Glasco and Rowlands.

CONCLUSION

In view of the foregoing remarks, Appellant's representative respectfully submits that the present application is in condition for allowance. Appellant's representative respectfully requests reconsideration of this application and that the application be passed to issue.

No additional fees should be due for this Reply Brief. In the event any fees are due in connection with the filing of this document, the Commissioner is authorized to charge those fees to Deposit Account No. 08-2025.

Respectfully submitted,

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EXHIBIT 1

for a memory line can migrate. See Glasco at para. [0047] and [0127]. Significantly, even during an eviction or write transaction, such as during a write back to memory, a given memory controller remains the serialization point for the memory line before, during and after writing back to memory. See Glasco at para. [0137] and [0127]. Since Glasco fails to teach that an ordering point can migrate from a node to memory, as recited in claim 1, Glasco consequently also fails to teach that memory would provide any acknowledgement to indicate that the ordering point has migrated from the first node to the memory, as recited in claim 1. For example, what basis exists for memory to provide an acknowledgement to an event that simply does not occur in the system of Glasco?

Additionally, the Office Action appears to have misconstrued the teachings Glasco by contending that the modified write back message described in Glasco is provided in response to an acknowledgement provided by the memory indicating that the ordering point has migrated from the first node to the memory. In contrast to the contention in the Office Action, Glasco teaches the modified line of memory must first be written back to memory before the line is invalidated if the directory entry indicates that the line is in the "dirty" state in any of the remote caches. See Glasco at para. [0116], lines 4 to 8, and para. [0126]. As discussed above, Glasco taken in whole or part, fails to teach that an ordering point migrate for data migrates to memory, such that there can be no broadcasting of a write-back message by the first node in response to the acknowledgement provided by the memory, as recited in claim 1. For the reasons stated above, Applicant respectfully requests reconsideration and allowance of claim 1.

In contrast to claim 2, Glasco fails to teach or suggest that a cache lines has associated state that defines the cache line as a cache ordering point for the data prior to employing the write-back transaction (of claim 1). As discussed with respect to claim 1, Glasco teaches that a